What is claimed is:

1. Device for processing data, comprising:

    a processor (1) for executing program routines, and

    a memory (2) for storing program routines to be executed
    by said processor (1), where

    at least a part of said memory (2) is arranged as a
    protected part (21) from which data can be read but
    which is protected against being written into, and

    said processor (1) is arranged to necessarily execute a
    program routine stored in said protected part of said
    memory upon start-up.

2. Device according to claim 1, wherein said processor (1)
    stores permanent start addresses (11) that are
    necessarily called upon start-up of said processor (1),
    where at least one of said start addresses points to
    said protected part (21) of said memory (2).

3. Device according to one of claims 1 or 2, wherein said
    protected part (21) of said memory (2) is a first part,
    and said memory further comprises a second part (22)
    into which data can be written, where the program
    routine from said protected part (21) executed by said
    processor (1) upon start-up comprises checking for
    changes in at least a part of the data contained in said
    second part (22).

4. Device according to claim 3, wherein said program
    routine from said protected part (21) executed by said
    processor (1) upon start-up comprises calculating a
    characteristic parameter for data being checked for
    changes and comparing said characteristic parameter

with a value stored in said second part (22) of said memory (2) at the time of writing said data being checked for changes into said second part (22) of said memory (2).

5. Device according to claim 4, wherein said characteristic parameter is a check sum.

6. Device according to one of claims 1 to 5, wherein said memory (2) comprises a plurality of memory devices (201, 202, 203), one (201) of which comprises said protected part, and the rest (202, 203) of which are arranged such that data may be written into them.

7. Device according to one of the preceding claims, wherein said protected area (21) is arranged such that a mechanism is provided such that after data is initially stored in said protected part (21), any subsequent writing of data into said protected part (21) is blocked.

8. Device according to claim 7, wherein said protected area (21) is arranged such that the process for storing data therein comprises:
writing (S1) data into said protected part (21) via a write line, and
sending (S2) a signal to said protected part in response to which said write line is permanently interrupted.

9. Device according to claim 8, wherein said write line is a fusable link.

10. Device according to one of claims 1 to 7, wherein said memory (1) comprises a finite state machine, said finite state machine defining a state which protects said protected part from being written into.

11. Device according to one of the preceding claims, wherein said memory (2) comprise one or more of an EEPROM, a flash memory device, and a flash memory device emulating an EEPROM.

12. Device according to one of the preceding claims, wherein said memory (2) comprises a memory chip (5) having electrical contacts (51) for being connected with a circuit board (6) that are arranged such that said electrical contacts (51) are covered by said memory chip (5) when said memory chip (5) is mounted on said circuit board (6).

13. Device according to claim 12, wherein said electrical contacts (51) are provided in a ball-grid-array.

14. Communication device comprising a device for processing data according to one of claims 1 to 13.

15. Communication device according to claim 14, wherein said communication device is a mobile telephone.

16. Communication device according to claim 14, wherein said communication device is a bluetooth communication device.

17. Method for controlling a data processing device having a processor (1) for executing program routines and a memory (2) for storing program routines to be executed by said processor (1), where at least a part of said memory (2) is arranged as a protected part (21) from which data can be read but which is protected against being written into, comprising:
letting (S4) said processor (1) necessarily execute a program routine stored in said protected part of said memory upon start-up (S3).

18. Method according to claim 17, wherein said processor stores permanent start addresses that are necessarily called upon start-up of said processor, where at least one of said start addresses points to said protected part of said memory.

19. Method according to one of claims 17 or 18, wherein said protected part of said memory is a first part, and said memory further comprises a second part into which data can be written, where the program routine from said protected part executed by said processor upon start-up comprises checking for changes in at least a part of the data contained in said second part.

20. Method according to claim 19, wherein said program routine from said protected part executed by said processor upon start-up comprises calculating a characteristic parameter for data being checked for changes, and comparing said characteristic parameter with a value stored in said second part of said memory at the time of writing said data being checked for changes into said second part of said memory.

21. Method according to claim 20, wherein said characteristic parameter is a check sum.

22. Method according to one of claims 17 to 21, wherein said memory comprises a plurality of memory devices, one of which comprises said protected part, and the rest of which are arranged such that data may be written into them.

23. Method according to one of claims 17 to 22, wherein said protected area is arranged such that a mechanism is provided such that after data is initially stored in said protected part, any subsequent writing of data into said protected part may be blocked.

24. Method according to claim 23, wherein said protected area is arranged such that the process for storing data therein comprises:

writing data into said protected part via a write line, and

sending a signal to said protected part in response to which said write line is permanently interrupted.

25. Method according to claim 24, wherein said write line is a fusable link.

26. Method according to one of claims 17 to 23, wherein said memory (1) comprises a finite state machine, said finite state machine defining a state which protects said protected part from being written into.

27. Method according to one of claims 17 to 26, wherein said memory comprise one or more of an EEPROM, a flash memory device, and a flash memory device emulating an EEPROM.

28. Method according to one of claims 17 to 27, wherein said memory comprises a memory chip having electrical contacts for being connected with a circuit board that are arranged such that said electrical contacts are covered by said memory chip when said memory chip is mounted on said circuit board.

29. Method according to claim 28, wherein said electrical contacts are provided in a ball-grid-array.

30. A medium readable by a data processing device, having a program recorded thereon, where the program is to make the data processing device execute the method of one of claims 17 to 29.